CLAIMS

What is claimed is:

1. An oscillation synthesizer comprises:

phase and frequency detector operably coupled to generate a charge up signal when phase of a reference oscillation leads phase of a feedback oscillation or when frequency of the reference oscillation leads frequency of the feedback oscillation, to generate a charge down signal when the phase of the reference oscillation lags the phase of the feedback oscillation or when the frequency of the reference oscillation lags the frequency of the feedback oscillation;

charge pump operably coupled to produce a positive current in response to the charge up signal and to produce a negative current in response to the charge down signal;

loop filter operably coupled to generate a control voltage based on the positive current and negative current;

voltage controlled oscillator operably coupled to generate an output oscillation based on the control voltage; and

divider module operably coupled to produce the feedback oscillation from the output oscillation based on a divider value, wherein the divider module includes:

plurality of flip-flops interoperably coupled to produce the divider value based on a control signal; and

logic circuit operably coupled to produce the control signal based on divider select signals, wherein each of the plurality of flip-flops includes:

first differential latch module operably coupled to produce a differential latched signal based on a differential flip-flop input signal; and

second differential latch module operably coupled to produce a differential flip-flop output based on the differential latched signal, wherein the first and second differential latch modules each includes:

sample transistor section operably coupled to sample, when coupled to a supply voltage, a differential input signal to produce a sampled differential input signal;

hold transistor section operably coupled to latch, when coupled to the supply voltage, the sampled differential input signal thereby producing a latched differential signal;

first gating circuit operable to couple the sample transistor section to the supply voltage in accordance with a first clocking logic operation and a second clocking logic operation, wherein the first clocking logic operation is based on a negative leg and a positive leg of a differential clock signal, and wherein the second clocking logic operation is based on the negative leg and the positive leg of the differential clock signal; and

second gating circuit operable to couple the hold transistor section to the supply voltage in accordance with a third clocking logic operation and a fourth clocking logic operation, wherein the third clocking logic operation is based on the negative leg and the positive leg of the differential clock signal, and wherein the fourth clocking logic operation is based on the negative leg and the positive leg of the differential clock signal.

2. The oscillation synthesizer of claim 1, wherein the first gating circuit further comprises:

first enable transistor operable to couple the sample transistor section to a first potential of the supply voltage based on the positive leg of the differential clock signal;

second enable transistor operable to couple the sample transistor section to a second potential of the supply voltage based on the negative leg of the differential clock signal;

first clock skew correction module operably coupled in parallel with the first enable transistor, wherein the first clock skew correction module couples the sample transistor section to the first potential based on a first logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in parallel with the second enable transistor, wherein the second clock skew correction module couples the sample transistor section to the second potential based on a second logic function of the positive and negative legs of the differential clock signal.

3. The oscillation synthesizer of claim 2, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the first potential, the drain is coupled to the sample transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NAND gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

4. The oscillation synthesizer of claim 2, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the second potential, the drain is coupled to the sample transistor section, and the gate is coupled to receive a second clock skew correction signal; and

NOR gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

5. The oscillation synthesizer of claim 1, wherein the second gating circuit further comprises:

first enable transistor operable to couple the hold transistor section to a first potential of the supply voltage based on the negative leg of the differential clock signal;

second enable transistor operable to couple the hold transistor section to a second potential of the supply voltage based on the positive leg of the differential clock signal;

first clock skew correction module operably coupled in series with the first enable transistor, wherein the first clock skew correction module couples the hold transistor section to the first potential based on a second logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in series with the second enable transistor, wherein the second clock skew correction module couples the hold transistor section to the second potential based on a first logic function of the positive and negative legs of the differential clock signal.

6. The oscillation synthesizer of claim 5, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NOR gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

7. The oscillation synthesizer of claim 5, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section and the gate is coupled to receive a second clock skew correction signal; and

NAND gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

8. The oscillation synthesizer of claim 1, wherein the first gating circuit further comprises:

first enable transistor operable to couple the sample transistor section to a first potential of the supply voltage based on the positive leg of the differential clock signal;

second enable transistor operable to couple the sample transistor section to a second potential of the supply voltage based on the negative leg of the differential clock signal;

first clock skew correction module operably coupled in series with the first enable transistor, wherein the first clock skew correction module couples the sample transistor section to the first potential based on a second logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in series with the second enable transistor, wherein the second clock skew correction module couples the sample transistor section to the second potential based on a first logic function of the positive and negative legs of the differential clock signal.

9. The oscillation synthesizer of claim 8, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NOR gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

10. The oscillation synthesizer of claim 8, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section and the gate is coupled to receive a second clock skew correction signal; and

NAND gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

11. The oscillation synthesizer of claim 1, wherein the second gating circuit further comprises:

first enable transistor operable to couple the hold transistor section to a first potential of the supply voltage based on the negative leg of the differential clock signal;

second enable transistor operable to couple the hold transistor section to a second potential of the supply voltage based on the positive leg of the differential clock signal;

first clock skew correction module operably coupled in parallel with the first enable transistor, wherein the first clock skew correction module couples the hold transistor section to the first potential based on a first logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in parallel with the second enable transistor, wherein the second clock skew correction module couples the hold transistor section to the second potential based on a second logic function of the positive and negative legs of the differential clock signal.

12. The oscillation synthesizer of claim 11, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the first potential, the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NAND gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

13. The oscillation synthesizer of claim 11, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the second potential, the drain is coupled to the hold transistor section, and the gate is coupled to receive a second clock skew correction signal; and

NOR gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

14. An integrated circuit radio comprises:

a transmitter section operably coupled to convert outbound data into outbound radio frequency (RF) signals based on a transmitter local oscillation;

a receiver section operably coupled to convert inbound RF signals into inbound data based on a receiver local oscillation;

local oscillation module operably coupled to produce the transmitter and receiver local oscillations, wherein the local oscillation module includes:

phase and frequency detector operably coupled to generate a charge up signal when phase of a reference oscillation leads phase of a feedback oscillation or when frequency of the reference oscillation leads frequency of the feedback oscillation, to generate a charge down signal when the phase of the reference oscillation lags the phase of the feedback oscillation or when the frequency of the reference oscillation lags the frequency of the feedback oscillation;

charge pump operably coupled to produce a positive current in response to the charge up signal and to produce a negative current in response to the charge down signal;

loop filter operably coupled to generate a control voltage based on the positive current and negative current;

voltage controlled oscillator operably coupled to generate an output oscillation based on the control voltage, wherein the transmitter and receiver local oscillations are based on the output oscillation; and

divider module operably coupled to produce the feedback oscillation from the output oscillation based on a divider value, wherein the divider module includes:

plurality of flip-flops interoperably coupled to produce the divider value based on a control signal; and

logic circuit operably coupled to produce the control signal based on divider select signals, wherein each of the plurality of flip-flops includes:

first differential latch module operably coupled to produce a differential latched signal based on a differential flip-flop input signal; and

second differential latch module operably coupled to produce a differential flip-flop output based on the differential latched signal, wherein the first and second differential latch modules each includes:

sample transistor section operably coupled to sample, when coupled to a supply voltage, a differential input signal to produce a sampled differential input signal;

hold transistor section operably coupled to latch, when coupled to the supply voltage, the sampled differential input signal thereby producing a latched differential signal;

first gating circuit operable to couple the sample transistor section to the supply voltage in accordance with a first clocking logic operation and a second clocking logic operation, wherein the first clocking logic operation is based on a negative leg and a positive leg of a differential clock signal, and wherein the second clocking logic

operation is based on the negative leg and the positive leg of the differential clock signal; and

second gating circuit operable to couple the hold transistor section to the supply voltage in accordance with a third clocking logic operation and a fourth clocking logic operation, wherein the third clocking logic operation is based on the negative leg and the positive leg of the differential clock signal, and wherein the fourth clocking logic operation is based on the negative leg and the positive leg of the differential clock signal.

15. The integrated circuit radio of claim 14, wherein the first gating circuit further comprises:

first enable transistor operable to couple the sample transistor section to a first potential of the supply voltage based on the positive leg of the differential clock signal;

second enable transistor operable to couple the sample transistor section to a second potential of the supply voltage based on the negative leg of the differential clock signal;

first clock skew correction module operably coupled in parallel with the first enable transistor, wherein the first clock skew correction module couples the sample transistor section to the first potential based on a first logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in parallel with the second enable transistor, wherein the second clock skew correction module couples the sample transistor section to the second potential based on a second logic function of the positive and negative legs of the differential clock signal.

16. The integrated circuit radio of claim 15, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the first potential, the drain is coupled to the sample transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NAND gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

17. The integrated circuit radio of claim 15, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the second potential, the drain is coupled to the sample transistor section, and the gate is coupled to receive a second clock skew correction signal; and

NOR gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

18. The integrated circuit radio of claim 14, wherein the second gating circuit further comprises:

first enable transistor operable to couple the hold transistor section to a first potential of the supply voltage based on the negative leg of the differential clock signal;

second enable transistor operable to couple the hold transistor section to a second potential of the supply voltage based on the positive leg of the differential clock signal;

first clock skew correction module operably coupled in series with the first enable transistor, wherein the first clock skew correction module couples the hold transistor

section to the first potential based on a second logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in series with the second enable transistor, wherein the second clock skew correction module couples the hold transistor section to the second potential based on a first logic function of the positive and negative legs of the differential clock signal.

19. The integrated circuit radio of claim 18, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NOR gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

20. The integrated circuit radio of claim 18, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section and the gate is coupled to receive a second clock skew correction signal; and

NAND gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

21. The integrated circuit radio of claim 14, wherein the first gating circuit further comprises:

first enable transistor operable to couple the sample transistor section to a first potential of the supply voltage based on the positive leg of the differential clock signal;

second enable transistor operable to couple the sample transistor section to a second potential of the supply voltage based on the negative leg of the differential clock signal;

first clock skew correction module operably coupled in series with the first enable transistor, wherein the first clock skew correction module couples the sample transistor section to the first potential based on a second logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in series with the second enable transistor, wherein the second clock skew correction module couples the sample transistor section to the second potential based on a first logic function of the positive and negative legs of the differential clock signal.

22. The integrated circuit radio of claim 21, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NOR gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

23. The integrated circuit radio of claim 21, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the drain is coupled to the hold transistor section and the gate is coupled to receive a second clock skew correction signal; and

NAND gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.

24. The integrated circuit radio of claim 14, wherein the second gating circuit further comprises:

first enable transistor operable to couple the hold transistor section to a first potential of the supply voltage based on the negative leg of the differential clock signal;

second enable transistor operable to couple the hold transistor section to a second potential of the supply voltage based on the positive leg of the differential clock signal;

first clock skew correction module operably coupled in parallel with the first enable transistor, wherein the first clock skew correction module couples the hold transistor section to the first potential based on a first logic function of the positive and negative legs of the differential clock signal; and

second clock skew correction module operably coupled in parallel with the second enable transistor, wherein the second clock skew correction module couples the hold transistor section to the second potential based on a second logic function of the positive and negative legs of the differential clock signal.

25. The integrated circuit radio of claim 24, wherein the first clock skew correction module further comprises:

a P-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the first potential, the drain is coupled to the hold transistor section, and the gate is coupled to receive a first clock skew correction signal; and

NAND gate operably coupled to produce the first clock skew correction signal based on the negative and positive legs of the differential clock signal.

26. The integrated circuit radio of claim 24, wherein the second clock skew correction module further comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source is coupled to the second potential, the drain is coupled to the hold transistor section, and the gate is coupled to receive a second clock skew correction signal; and

NOR gate operably coupled to produce the second clock skew correction signal based on the negative and positive legs of the differential clock signal.